

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Patent Application of:)

Zorian et al.)

Examiner: Not Yet Assigned

Application No.: Not Yet Assigned)

Art Unit: Not Yet Assigned

Filed: Herewith)

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Date of Deposit: September 16, 2003For: VARIOUS METHODS AND)
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September 16, 2003
(Date signed)Assistant Commissioner for Patents
Washington, D.C. 20231INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449 together with copies of the documents cited on that form. It is respectfully requested that the cited documents be considered and that the enclosed copy of Information Disclosure Citation Form PTO-1449 be initialed by the Examiner to indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):

 X 37 C.F.R. §1.97(b).

 37 C.F.R. §1.97(c). If so, then enclosed with this Information Disclosure Statement is one of the following:

 A statement pursuant to 37 C.F.R. §1.97(e) or

 A check for \$180.00 for the fee under 37 C.F.R. § 1.17(p).

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- (1) A statement pursuant to 37 C.F.R. §1.97(e); and
- (2) A check for \$180.00 for the fee under 37 C.F.R. §1.17(p) for submission of the Information Disclosure Statement.

If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 9-16, 2003



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Substitute for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known		
				Application Number	N/A	
				Filing Date	Herewith	
				First Named Inventor:	Zorian	
				Art Unit	N/A	
				Examiner Name	Unassigned	
				Attorney Docket Number	04640.P019	
Sheet	1	of		2		
U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Document Number		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)				
		US-	5,513,318	04/30/1996	Van de Goor, et al.	
		US-	5,960,009	09/28/1999	Gizopoulos, et al.	
		US-	5,978,935	11/02/1999	Kim, et al.	
		US-	5,978,947	11/02/1999	Kim, et al.	
		US-	6,330,696 B1	12/11/2001	Zorian, et al.	
		US-	6,397,349 B2	05/28/2002	Higgins, et al.	
		US-	6,237,123 B1	05/22/2001	Kim, et al.	
		US-	6,205,564 B1	05/20/2001	Kim, et al.	
		US-	6,085,334	07/04/2000	Giles, et al.	
		US-	6,317,846 B1	11/13/2001	Higgins, et al.	
		US-	5,570,374	10/29/1996	Yau, et al.	
		US-				
		US-				
		US-				
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FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SENT FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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Substitut for Form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	N/A
				Filing Date	Herewith
				First Named Inventor:	Zorian
				Art Unit	N/A
				Examiner Name	Unassigned
Sheet	2	of	2	Attorney Docket Number	04640.P019
NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published			T ²
		Yervant Zorian: "System-Chip Test Strategies" (Tutorial): DAC 1998: 752-757.			
		Ilyoung Kim, Yervant Zorian, Goh Komoriya, Hai Pham, Frank P. Higgins, Jim L. Lewandowski: "Built-in Self-Repair for Embedded High Density SRAM." ITC 1998: 1112-1119			
		Yervant Zorian, Erik Jan Marinissen, Sujit Dey: "Testing Embedded-Core Based System Chips." ITC 1998: pages 1-14			
		Yervant Zorian, Erik Jan Marinissen, "System Chip Test: How Will It Impact Your Design?", DAC, 2000, pages 1-6.			
		Monica Lobetti Bodoni, Alfredo Benso, Silvia Chiusano, Stefano DiCarlo, Giorgio DiNatale, Paolo Prinetto, "An Effective Distributed BIST Architecture for RAMs," pages 1-6, IEEE European Test Workshop, 2000.			
		Chauchin Su, Shih-Ching Hsiao, Hau-Zen Zhau, Chung-Len Lee, "A Computer Aided Engineering System for Memory BIST," DAC, 2001 pages 1-4.			
		Yervant Zorian, "Embedding Infrastructure IP for SOC Yield Improvement," June 2002, 709-712.			
		Praveen Parvathala, Kailas Maneparambil, William Lindsay, "FRITS – A Microprocessor Functional BIST Method," ITC, Mar. 2002, pages 590-598.			
		TechWeb definition, AUTHOR UNKNOWN, scan technology, copyright 1981-2001, 1 page.			
		S. Shoukourian, V. Vardanian, Y. Zorian, "An Approach for Evaluation of Redundancy Analysis Algorithms," The Proceedings of IEEE Int. Workshop on Memory Technology, Design and Testing, 2001.			
		D.K. Bhavsar, "An Algorithm for Row-Column Self-Repair of RAMs and its Implementation in the Alpha 21264," Proc. ITC'1999, pp. 311-318.			
		T. Kawagoe, J. Ohtani, M. Niuro, T. Oishi, M. Hamada, H. Hidaka, "A Built-In Self-Repair Analyzer (CRESTA) for Embedded DRAMs," Proc. ITC'2000, pp. 567-574.			

Examiner Signature		Date Considered	
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